REMARKS

By this Amendment, Applicant has canceled claim 6, and amended claims 1, 8 and 17-19. Claims 9-16 have been withdrawn from consideration. Claims 1-5, 7, 8 and 17-19 are pending in the application. In view of the above amendments and the following remarks, favorable reconsideration in this application is respectfully requested.

The Examiner rejected claims 8 and 17-19 under 35 U.S.C. 112, second paragraph, as being indefinite and failing to conform to U.S. practice, and rejected claim 18 under 35 U.S.C. 112, fourth paragraph. The Examiner also rejected claims 17-19 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,968,264 to Iida et al. ("Iida") in view of U.S. Patent No. 4,193,783 to Matsushita.

By this Amendment, Applicant has amended claims 8 and 17-19 to bring such claims into conformity with 35 U.S.C. 112, second paragraph. With respect to the rejection of claim 18 under the fourth paragraph of 35 U.S.C. 112, while Applicant has amended claims 17-19 to overcome the rejection, Applicant notes that examples from the specification cannot be properly read into the claims, i.e., the phrase "a predetermined thermal history" in claim 17 is not limited to the specific example given in the specification of such a history.

The Examiner rejected claims 1-3, 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,376,657 to Nagasawa et al. ("Nagasawa"), and further rejected claim 4 as being unpatentable over Nagasawa in view of U.S. Patent No. 5,352,615 to Limb et al, claim 5 as being unpatentable over Nagasawa in view of U.S. Patent No. 4,429,047 to Jastrzebski et al along with U.S. Patent No. 5,882,989 to Falster, claims 17-19 as being

unpatentable over U.S. Patent No. 5,968,264 to Iida et al ("Iida") in view of U.S. Patent No. 4,193,783 to Matsushita, and claim 8 as being unpatentable over Iida in view of Matsushita and further in view of Nagasawa.

As set forth in amended claim 1, the present invention is directed to a method of treating a wafer thermally to remove defects contained in single crystalline semiconductor, comprising the steps of carrying out a heat treatment on the wafer at a temperature equal to or higher than 1200 °C, and then carrying out an RTP annealing on the wafer at a temperature equal to or lower than 800°C for a period having a duration of two minutes or less.

While Nasagawa discloses a second heat treatment, the teaching requires that the second treatment be for "more than one hour, preferably for 16 hours" (see the Abstract); this clearly does not include a rapid thermal annealing of "2 minutes or less". The Examiner's statement that "the limitation of 2 minutes or less does not have an upper bound" is incorrect in that "2 minutes" is clearly the upper bound. The "comprising" language of the claim cannot be read to negate a specified element of the range that limits the duration of the rapid thermal annealing to the period of 2 minutes, or some amount of time less than 2 minutes.

Nor does Nasagawa suggest such a rapid heat treatment, instead explicitly teaching that the second heat treatment requires in excess of one hour, and preferably a period of 16 hours. Such a range is clearly in significant excess of "2 minutes or less" and teaches away from such a brief treatment.

For at least the foregoing reasons, claims 1 and 8 are neither taught nor suggested by the prior art, but are patentable thereover. Favorable reconsideration is requested. Claims 2-5 and 7 are also in condition for allowance as claims properly dependent on an allowable base claim. Favorable reconsideration and allowance thereof is requested.

As set forth in amended claim 17, the present invention is also directed to a method of growing an ingot comprising the steps of accelerating a speed of growing from a melt-down silicon to a single crystalline silicon ingot, maintaining a temperature gradient distribution from a central part to a circumferential part of the ingot at a growing interface between the melt-down silicon and the ingot grown by crystallization, forming an OiSF ring at the circumferential part by moving the OiSF ring from a center of a single crystalline semiconductor growth axis to a circumference, and extending an area in which delta (Oi) is increased as compared to that of other areas, wherein the delta (Oi) is a difference between an initial oxygen concentration and oxygen concentration after heat treatment with a thermal history.

Iida is directed to growing a single crystal ingot which includes a neutral region. In contrast, the present invention as set forth in claim 17 is directed to a method of forming wafers which include a vacancy rich region. Instead of forming wafers including the "A" region as identified in Figure 1, with the present invention wafers are made from only the "B" region, which is a patentable improvement over the prior art. Favorable reconsideration and allowance of claim 17, as well as claims 18 and 19 dependent thereon, is requested.

Attached hereto is a marked-up version of the changes made to the application by the current amendment. The attached pages are captioned "Version with Markings to Show Changes Made".

Should the Examiner have any questions or comments, the Examiner is cordially invited to telephone the undersigned attorney so that the present application can receive an early Notice of Allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 6 has been canceled and claims 1, 8 and 17-19 have been amended as follows:

1. (Amended) A method of treating a wafer thermally to remove defects contained in single crystalline semiconductor, the method comprising the steps of:

carrying out a [first] heat treatment on the wafer at a temperature equal to or higher than 1200 °C; and

carrying out a [second heat treatment] rapid thermal annealing on the wafer at a temperature equal to or lower than 800°C for a period having a duration of two minutes or less.

8. (Amended) A method of producing a semiconductor wafer, comprising the steps of:

producing a single crystalline semiconductor ingot by removing an OiSF ring by means of moving the OiSF ring from a center of a single crystalline semiconductor growth axis to a circumference and by extending a first area and a second area in which delta (Oi) as oxygen concentration difference between initial oxygen concentration and oxygen concentration after heat treatment in N_2 ambience at 1000 °C for 64 hours, is [more greatly] increased more than other areas;

providing a wafer by slicing the single crystalline semiconductor ingot;

carrying out a [first] heat treatment on the wafer at a temperature equal to or higher than 1200 °C; and

carrying out a [second heat treatment] rapid thermal annealing on the wafer at a temperature equal to or lower than 800°C for a period having a duration of two minutes or less.

17. (Amended) A method of growing an ingot, comprising the steps of:

accelerating a speed of growing from a melt-down silicon to a single crystalline silicon ingot;

maintaining a temperature gradient distribution from a central part to a circumferential part of the ingot at a growing interface between the melt-down silicon and the ingot grown by crystallization;

forming an OiSF ring at the circumferential part by moving the OiSF ring from a center of a single crystalline semiconductor growth axis to a circumference; and

extending an area in which delta (Oi) is [greatly] increased as compared to that of other areas, wherein the delta (Oi) is a difference between an initial oxygen concentration and oxygen concentration after heat treatment with a [predetermined] thermal history.

18. (Amended) The method of growing an ingot according to claim 17, wherein the heat treatment with the [predetermined] thermal history is carried out at 1000°C for 64 hours in a N_2 ambience.

19. (Amended) The method of growing an ingot according to claim 17, wherein the area in which delta (Oi) is [greatly] increased is formed to occupy 20 to 90% of a diameter of the ingot.